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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,472	11/26/2003	Dean A. Klein	MTIPAT.024DV2	9869

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EXAMINER

GU, SHAWN X

ART UNIT PAPER NUMBER

2189

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/724,472	Applicant(s) KLEIN, DEAN A.	
	Examiner Shawn Gu	Art Unit 2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 November 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-51 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-10,12-15,17-21,23-28,30,31,33-39 and 41-49 is/are rejected.
- 7) ☒ Claim(s) 2,11,16,22,29,32,40,50 and 51 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>11/26/03</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Priority

This Office Action is responsive to the application filed on 26 November 2003.

Acknowledgment is made of applicant's claim for domestic priority under 35 U.S.C. 120.

Claims 1-51 are presented for examination.

Claims 1-51 are pending.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 26 November 2003 was filed after the mailing date of the application on 26 November 2003. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir.

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1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1, 4, 9, 10, 12, 13, 15, 20, 21, 24, 30, 31, 33, 34, 41, 42, 43, 46 and 49 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 4-7, 10, 11, 14-16, 21, 24, 26, 28, 29, 34, 36, 38-40, 45, 49, 50, and 52 of copending Application No.10733896. Although the conflicting claims are not identical, they are not patentably distinct from each other because the claimed invention in the present application is an obvious derivation from the co-pending application, as both of the instant invention and the co-pending applications describe reading, shifting, and storing a cache line in a cache memory using barrel shifter, wherein the cache memory is associated with a main memory comprising a DRAM and the cache comprising a Level 1 cache.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 112

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The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3, 23, 33, 35, and 45 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claims 3, 23, 35, and 45, it is unclear to the Examiner if the capacity is referring to full storage capacity, minimum capacity under certain conditions, or the ability to drive a certain number of signal lines connected to the register or means for storing data. The Examiner is reviewing the application in light of the first interpretation.

As for claim 33, it is unclear to the Examiner if the "entire cache line" is a cache line in the data memory in the claim, or is from another source not cited in the claim. The Examiner is rejecting the claim in light of the former interpretation.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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Claims 21 and 42 are rejected under 35 U.S.C 102(b) as being unpatentable over Groves [5,222,225] (hereinafter "Groves").

As for claim 21, Groves teaches a method of reassigning data from a first memory location to a second memory location (Col 5, Lines 61-68) comprising:

reading a cache (Fig 1, 20 Memory; Col 3, Line 68; Col 4, Line 1) line containing at least a portion of a data string from a data cache (Col 6, Lines 3-30);

shifting the cache line a selected amount (Col 6, Lines 3-30); and

storing the shifted cache line in the data cache (Col 6, Lines 31-48).

As for claim 42, it is clear the functions of claim 21 are performed by a processor (Fig 1), which further comprises the means for storing data shifted out of the cache line (Fig 2C, 18B Memory Bus and 22B Byte Rotate; Col 6, Lines 12-30; a rotator stores data shifted out of one end back to the other end).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 8, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Groves, further in view of Tran [5,900,012] (hereinafter "Tran").

As for claim 1, Groves teaches a method for moving a data string within a cache memory system, the method comprising:

reading a cache line from a data cache (Fig 1, 20 Memory; Col 3, Line 68; Col 4, Line 1), the cache line containing at least a portion of a data string (Col 6, Lines 3-30) and having a starting source address (Col 8, Lines 13-15);

shifting the cache line a selected amount (Col 6, Lines 3-30);

storing the shifted cache line in a first destination cache line in the data cache, the shifted cache line having a starting destination address (Col 6, Lines 31-48).

Although Groves does not specifically disclose modifying a cache tag value associated with the first destination cache line, Tran teaches a method for a cache system where a cache line is moved from its original location in the cache to first destination cache line (Col 6, Lines 26-39), and the cache tag value associated with the first destination cache line is modified to reflect a location of the data in a main memory (Col 6, Lines 39-43), in order to complete the move of a cache line in accordance to the operational principle of a cache memory (tag value of a cache line must correctly reflect the corresponding main memory location in order to maintain cache to memory coherency). Therefore it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that Groves cache memory system could have an

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associated main memory for larger storage capacity than the cache memory (Tran, Col 1, Lines 36-39), and the described feature in Tran's method can be incorporated into Grove's method in order to maintain cache to main memory data coherency.

As for claim 8, the first destination cache line is replaced by the shifted cache line, and it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that data stored in the first destination cache line needs to be written to the main memory prior to the data string move if the first destination cache line contains updated data in order to maintain data coherency.

It is clear claim 28 is already substantially described in the above claims.

Claims 4, 5, 6, 9, 12, 14, 15, 17, 19, 25, 26, 30, 33, 34, 36, 37, 41, 44, 46, and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Groves and Tran, further in view of Pogue et al. [4,920,483] (hereinafter Pogue).

As for claims 12 and 33, Groves already substantially discloses the claims in further view of Tran, as described above in claim 1, but does not particularly pointed out that the entire cache line is shifted in a single processor cycle by a barrel shifter. However, Pogue teaches a memory system comprising a barrel shifter that shifts a plurality of bits in a single processor cycle, in order to save the number of cycles used for the shift operation. Therefore it would have been obvious to one ordinarily skilled in

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the art at the time of the Applicant's invention that a barrel shifter can be used in Groves' cache memory to facilitate shifting of the cache line in a single processor cycle in order to save processing time.

As for claim 4, the claim is already substantially disclosed in claims 1, 12, and 33 as described above.

As for claims 5, 14, 25, 36, and 44, Groves teaches that the selected amount to be shifted is an amount equal to a change in offset between the starting source address and the starting destination address (Col 6, Lines 31-42).

As for claims 6, 17, 26, 37, and 47, the first destination cache line is replaced by the shifted cache line, and it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that when a cache entry is modified, its dirty bit is set to indicate the cache line as having been modified, in order to write back the updated data to the associated main memory when needed in order to maintain data coherency.

As for claims 9, 30, 41, Tran teaches the main memory in the cache memory disclosed by Groves in further view of Tran and Pogue is a DRAM circuit (Col 1, Lines 36-39).

As for claims 15, 34, and 46, Groves teaches a register coupled to the shifter for storing data shifted out of the shifter during shift operations (Col 6, Lines 3-42).

As for claim 19, it is already substantially disclosed in the above claims.

Claims 7, 10, 18, 20, 27, 31, 38, 39, 48, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Groves, in combination with Tran and Pogue, in further view of Papworth et al. [5,404,473] (hereinafter "Papworth").

As for claims 7, 18, 27, 38, and 48, Papworth teaches that its method performs a snoop cycle in order to monitor data and address traffic for values in the cache to avoid retrieving outdated data (Col 5, Lines 24-33). Therefore it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that Groves' cache memory, in further view of Tran and Pogue, could perform a snoop cycle to monitor data and address traffic for values in the cache.

As for claims 10, 20, 31, 39, and 49, Papworth teaches a processing system that handles string operations which comprises a Level 1 cache, in order to improve processing speed (Col 6, Lines 5-8). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that Groves' cache memory in further view of Tran and Pogue, can incorporate a Level 1 cache in order to improve processing speed.

Allowable Subject Matter

Claims 2, 11, 16, 22, 29, 32, 40, 50, and 51 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

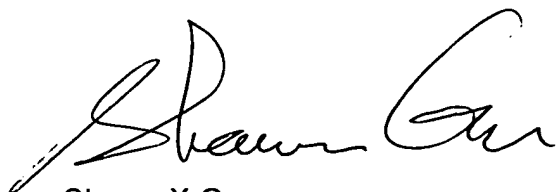
Claims 3, 23, 35, and 45 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claims and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Shawn X Gu
Assistant Examiner
Art Unit 2189



MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER

1 December 2005